Clean copy of allowed claims

1. A method for testing an integrated circuit, comprising:

providing a stimulus to a test bench;

providing a device model corresponding to the integrated circuit to the test bench;

in response to applying the stimulus to the device model through the test bench, generating captured simulation, the captured simulation comprising strobe timing information, opcode information, mixed signal information, and internal memory content information;

automatically generating tester software corresponding to the integrated circuit using the captured simulation;

generating a virtual test software;

testing the device model of the integrated circuit and debugging and verifying the tester software using the virtual test software; and

testing the integrated circuit using the tester software.

2. (Cancelled).

3. The method of claim 1, wherein the captured simulation captures all communication through the test bench between the stimulus and the device model.

4. (Cancelled).

5. (Cancelled).

6. (Cancelled)..

7. The method of claim 1, wherein the stimulus comprises verification patterns, drivers, and monitors.

8. (Cancelled).

9. (Cancelled).

10. (Cancelled).

11. The method of claim 1, wherein the captured simulation further comprises information relating to directionality information, pin data information, masking information, comment information, and partial cyclized information.

12. A method for testing an integrated circuit, comprising:

generating a captured simulation in response to applying a stimulus to a device model of the integrated circuit, wherein the captured simulation comprises strobe timing information, opcode information, mixed signal information, and internal memory content information, the captured simulation generated in response to stimulus applied to the device model through a test bench;

generating data patterns based on strobe timing information, opcode information, mixed signal information, and internal memory content information, the data patterns capable of being retargettable for a plurality of post-processing tools;

generating a first formatted pattern file based on the data patterns;

automatically generating tester software corresponding to the integrated circuit using the first formatted pattern file;

testing the device model of the integrated circuit and debugging and verifying the tester software using virtual test software; and

testing the integrated circuit using the tester software in an automatic test equipment (ATE) tester.

13. (Cancelled).

14. The method of claim 12, wherein the captured simulation further comprises information relating to directionality information, pin data information, masking information, comment information, and partial cyclized information.

15. The method of claim 12, wherein the data patterns include cyclized patterns.

16. (Cancelled).

17. (Cancelled).

18. A testing system for testing an integrated circuit, comprising:

simulation means for generating a captured simulation in response to applying a stimulus to a device model of the integrated circuit;

first instruction means for receiving the captured simulation wherein the captured simulation comprises strobe timing information, opcode information, mixed signal information, and internal memory content information, the captured simulation generated in response to stimulus applied to a device model through a test bench;

second instruction means for generating data patterns based on strobe timing information, opcode information, mixed signal information, and internal memory content information, the data patterns capable of being retargettable for a plurality of post-processing tools;

third instruction means for generating a first formatted pattern file based on the data patterns;

fourth instruction means for automatically generating tester software corresponding to the integrated circuit using the first formatted pattern file;

fifth instruction means for testing the device model of the integrated circuit and debugging and verifying the tester software using a virtual test software; and

an automatic test equipment (ATE) tester for testing the integrated circuit using the tester software.

19. (Cancelled).

20. (Cancelled).

21. (Cancelled).

22. A testing system for testing an integrated circuit, comprising:

first instruction means for receiving a stimulus;

second instruction means for receiving a device model corresponding to an integrated circuit;

third instruction means for generating simulation parameters in response to applying the stimulus to the device model;

fourth instruction means for creating captured simulation based on the simulation parameters, the captured simulation comprising strobe timing information, opcode information, mixed signal information, and internal memory content information; and

fifth instruction means for automatically generating tester software corresponding to the integrated circuit using the captured simulation;

sixth instruction means for testing the device model of the integrated circuit and debugging and verifying the tester software using a virtual test software; and

an automated tester means for testing the integrated circuit using the tester software.

23. (Cancelled).

24. The testing system of claim 22, wherein the captured simulation captures all communication between the stimulus and the device model through a standard reusable test bench.

25. The testing system of claim 24, wherein all communication with the device model occurs through the standard reusable test bench.

26. (Cancelled).

27. The testing system of claim 22, wherein the captured simulation comprises information relating to directionality information, pin data information, masking information, comment information, and partial cyclized information.